IN THE CLAIMS

1. (Original) A multi-layer structure for a semiconductor device, comprising:

a silicate interface layer; and

a high-k dielectric layer overlying the silicate interface layer.

2. (Original) The multi-layer structure of claim 1, wherein the silicate interface layer has a dielectric constant greater than that of silicon nitride.

3. (Original) The multi-layer structure of claim 1, wherein the high-k dielectric layer has a dielectric constant greater than that of the silicate interface layer.

4. (Original) The multi-layer structure of claim 1, wherein the silicate interface layer is formed of a metal silicate material ($M_{1-x}Si_xO_2$).

5. (Original) The multi-layer structure of claim 4, wherein x is approximately 0.30-0.99.

6. (Original) The multi-layer structure of claim 4, wherein the metal "M" is selected from the group consisting of hafnium (Hf), zirconium (Zr), tantalum (Ta), titanium (Ti) and aluminum (Al).

7. (Original) The multi-layer structure of claim 1, wherein the silicate interface layer is formed by an ALD technique, a MOCVD technique or a reactive sputtering technique.

8. (Original) The multi-layer structure of claim 1, wherein the silicate interface layer is formed to a thickness of approximately 5-10 angstroms.

9. (Original) The multi-layer structure of claim 1, wherein the high-k dielectric layer is a metal oxide layer.

10. (Original) The multi-layer structure of claim 9, wherein the metal oxide layer is an HfO_2 layer, a ZrO_2 layer, a Ta_2O_3 layer, an Al_2O_3 layer, a TiO_2 layer, an Y_2O_3 layer, or a BST layer, a PZT layer, or combinations thereof.

11. (Original) The multi-layer structure of claim 9, wherein the metal oxide layer is formed using an ALD technique, a MOCVD technique or a reactive sputtering technique.

12. (Original) The multi-layer structure of claim 9, wherein the silicate interface layer is formed of a metal silicate material, and wherein the metal of the silicate interface layer is the same as the metal of the metal oxide layer.

13. (Original) The multi-layer structure of claim 1, wherein the high-k dielectric layer comprises one or more ordered pairs of first and second layers.

14. (Original) The multi-layer structure of claim 13, wherein the first layer is formed of HfO_2, Ta_2O_3, Y_2O_3 or ZrO_2 and the second layer is formed of Al_2O_3.

15. (Original) The multi-layer structure of claim 13, wherein the first layer has a first fixed charge and the second layer has a second fixed charge opposite that of the first fixed charge.

16. (Original) The multi-layer structure of claim 13, wherein the thickness of the second layer is approximately one half the thickness of the first layer.

17. (Original) The multi-layer structure of claim 16, wherein the first layer is formed to a thickness of approximately 10 angstroms and the second layer is formed to a thickness of approximately 5 angstroms.

18. (Original) The multi-layer structure of claim 13, wherein a total thickness of the second layer is not more than approximately one third of the total thickness of the high-k dielectric layer.

19. (Previously presented) The multi-layer structure of claim 13, wherein the upper most layer of the high-k dielectric layer is Al_2O_3.

20. (Original) A multi-layer structure for a semiconductor device, comprising:

a silicate interface layer having a dielectric constant greater than that of silicon nitride; and

a high-k dielectric layer overlying the silicate interface layer,

wherein the high-k dielectric layer comprises one or more ordered pairs of first and second layers, and wherein the high-k dielectric layer has a dielectric constant greater than that of the silicate interface layer.

21. (Original) The multi-layer structure of claim 20, wherein the silicate interface layer is formed of a metal silicate material ($M_{1-x}Si_xO_2$), the metal "M" being selected from the group consisting of hafnium (Hf), zirconium (Zr), tantalum (Ta), titanium (Ti) and aluminum (Al).

22. (Original) The multi-layer structure of claim 20, wherein the first layer is formed of HfO_2, Ta_2O_3, Y_2O_3 or ZrO_2 and the second layer is formed of Al_2O_3.

23. (Original) The multi-layer structure of claim 20, wherein the thickness of the second layer is approximately one half the thickness of the first layer.

24. (Original) The multi-layer structure of claim 20, wherein a total thickness of the second layer is not more than approximately one third of the total thickness of the high-k dielectric layer.

25. (Previously presented) The multi-layer structure of claim 20, wherein the upper most layer of the high-k dielectric layer is Al_2O_3.

26. (Withdrawn) A method of forming a multi-layer structure for a semiconductor device, comprising:

forming a silicate interface layer; and

forming a high-k dielectric layer overlying the silicate interface layer.

27. (Withdrawn) The method of claim 26, wherein said forming the high-k dielectric layer comprises:

forming a first layer having a first predefined charge;

forming a second layer overlying the first layer, the second layer having a second predefined charge that is opposite that of the first layer.

28. (Withdrawn) The method of claim 27, wherein the first predefined charge is a negative fixed charge and the second predefined charge is a positive fixed charge.

29. (Withdrawn) The method of claim 27, which further comprises forming one or more first and second layers.

30. (Withdrawn) The method of claim 29, wherein the upper most layer of the high-k dielectric layer is Al_2O_3.

31. (Withdrawn) The method of claim 26, wherein said forming the high-k dielectric layer comprises:

forming a first layer having a first controlled thickness; and

forming a second layer overlying the first layer, the second layer having a second controlled thickness, wherein the first and second controlled thicknesses are in the range of approximately 2-60 angstroms.

32. (Withdrawn) The method of claim 31, wherein a total thickness of the second layer is not more than approximately one third of the total thickness of the high-k dielectric layer.

33. (Withdrawn) The method of claim 31, wherein the second layer is approximately one half the thickness of the first layer.

34. (Withdrawn) The method of claim 31, wherein the first layer is formed of HfO_2, Ta_2O_3, Y_2O_3 or ZrO_2 and the second layer is formed of Al_2O_3.

35. (Withdrawn) The method of claim 26, wherein the silicate interface layer is formed of a metal silicate material ($M_{1-x}Si_xO_2$).

36. (Withdrawn) The method of claim 35, wherein x is approximately 0.30-0.99, and wherein the metal "M" is selected from the group consisting of hafnium (Hf), zirconium (Zr), tantalum (Ta), titanium (Ti) and aluminum (Al).

37. (Withdrawn) The method of claim 26, wherein said forming the silicate interface layer is performed by an ALD technique, a MOCVD technique or a reactive sputtering technique.

38. (Withdrawn) The method of claim 26, wherein the silicate interface layer is formed to a thickness of approximately 5-10 angstroms.

39. (Withdrawn) The method of claim 26, wherein the high-k dielectric layer is a metal oxide layer selected from the group consisting of an HfO_2 layer, a ZrO_2 layer, a Ta_2O_3 layer, an Al_2O_3 layer, a TiO_2 layer, an Y_2O_3 layer, a BST layer, a PZT layer, and combinations thereof.

40. (Withdrawn) The method of claim 39, wherein the metal oxide layer is formed using an ALD technique, a MOCVD technique or a reactive sputtering technique.

41. (Withdrawn) The method of claim 39, wherein the silicate interface layer is formed of a metal silicate material, and wherein the metal of the silicate interface layer is the same as the metal of the metal oxide layer.

42. (Previously presented) A transistor comprising:
a substrate;
a silicate interface layer formed over the substrate; and
a high-k dielectric layer formed over the silicate interface layer;
a gate formed over the high-k dielectric layer; and
a source/drain region formed adjacent the gate.

43. (Original) The transistor of claim 42, wher in an upper most portion of the high-k dielectric layer is Al_2O_3, and wherein said gate comprises poly-silicon.

44. (Original) A non-volatile memory, comprising:
a substrate;
a floating gate overlying the substrate;
a silicate interface layer formed over the floating gate;
a high-k dielectric layer formed over the silicate interface layer; and
a control gate overlying the high-k dielectric layer.

45. (Previously presented) A capacitor for a semiconductor device, comprising;
a lower electrode;
a silicate interface layer formed over the lower electrode;
a high-k dielectric layer formed over the silicate interface layer; and
an upper electrode formed over the high-k dielectric layer.

46. (Previously presented) The multi-layer structure of claim 1, wherein the multi-layer is used for a capacitor between a lower electrode and an upper electrode.

47. (Previously presented) The multi-layer structure of claim 14, wherein the multi-layer is used for a capacitor between a lower electrode and an upper electrode.

48. (Previously presented) The multi-layer structure of claim 20, wherein the multi-layer is used for a capacitor between a lower electrode and an upper electrode.

49. (Previously presented) The multi-layer structure of claim 22, wherein the multi-layer is used for a capacitor between a lower electrode and an upper electrode.

50. (New) The transistor of claim 42, wherein the silicate interface layer is formed of a metal silicate material ($M_{1-x}Si_xO_2$), the metal "M" being selected from the group consisting of hafnium (Hf), zirconium (Zr), tantalum (Ta), titanium (Ti) and aluminum (Al).

51. (New) The transistor of claim 42, wherein the high-k dielectric layer comprises one or more ordered pairs of first and second layers, and wherein the first layer is formed of HfO_2, Ta_2O_3, Y_2O_3 or Zro_2 and the second layer is formed of Al_2O_3.

52. (New) The non-volatile memory of claim 44, wherein the silicate interface layer is formed of a metal silicate material ($M_{1-x}Si_xO_2$), the metal "M" being selected from the group consisting of hafnium (Hf), zirconium (Zr), tantalum (Ta), titanium (Ti) and aluminum (Al).

53. (New) The non-volatile memory of claim 44, wherein the high-k dielectric layer comprises one or more ordered pairs of first and second layers, and wherein the first layer is formed of HfO_2, Ta_2O_3, Y_2O_3 or Zro_2 and the second layer is formed of Al_2O_3.

54. (New) The capacitor of claim 45, wherein the silicate interface layer is formed of a metal silicate material ($M_{1-x}Si_xO_2$), the metal "M" being selected from the group consisting of hafnium (Hf), zirconium (Zr), tantalum (Ta), titanium (Ti) and aluminum (Al).

55. (New) The capacitor of claim 45, wherein the high-k dielectric layer comprises one or more ordered pairs of first and second layers, and, wherein the first layer is formed of HfO_2, Ta_2O_3, Y_2O_3 or Zro_2 and the second layer is formed of Al_2O_3.

56. (New) A capacitor, comprising:

a lower electrode;

a high-k dielectric layer overlying the silicate interface layer,

wherein the high-k dielectric layer comprises one or more ordered pairs of first and second layers, and wherein the high-k dielectric layer has a dielectric constant greater than that of the silicate interface layer; and

an upper electrode.

57. (New) The capacitor of claim 56, wherein the silicate interface layer is formed of a metal silicate material ($M_{1-x}Si_xO_2$), the metal "M" being selected from the group consisting of hafnium (Hf), zirconium (Zr), tantalum (Ta), titanium (Ti) and aluminum (Al).

58. (New) The capacitor of claim 56, wherein the first layer is formed of HfO_2, Ta_2O_3, Y_2O_3 or ZrO_2 and the second layer is formed of Al_2O_3.